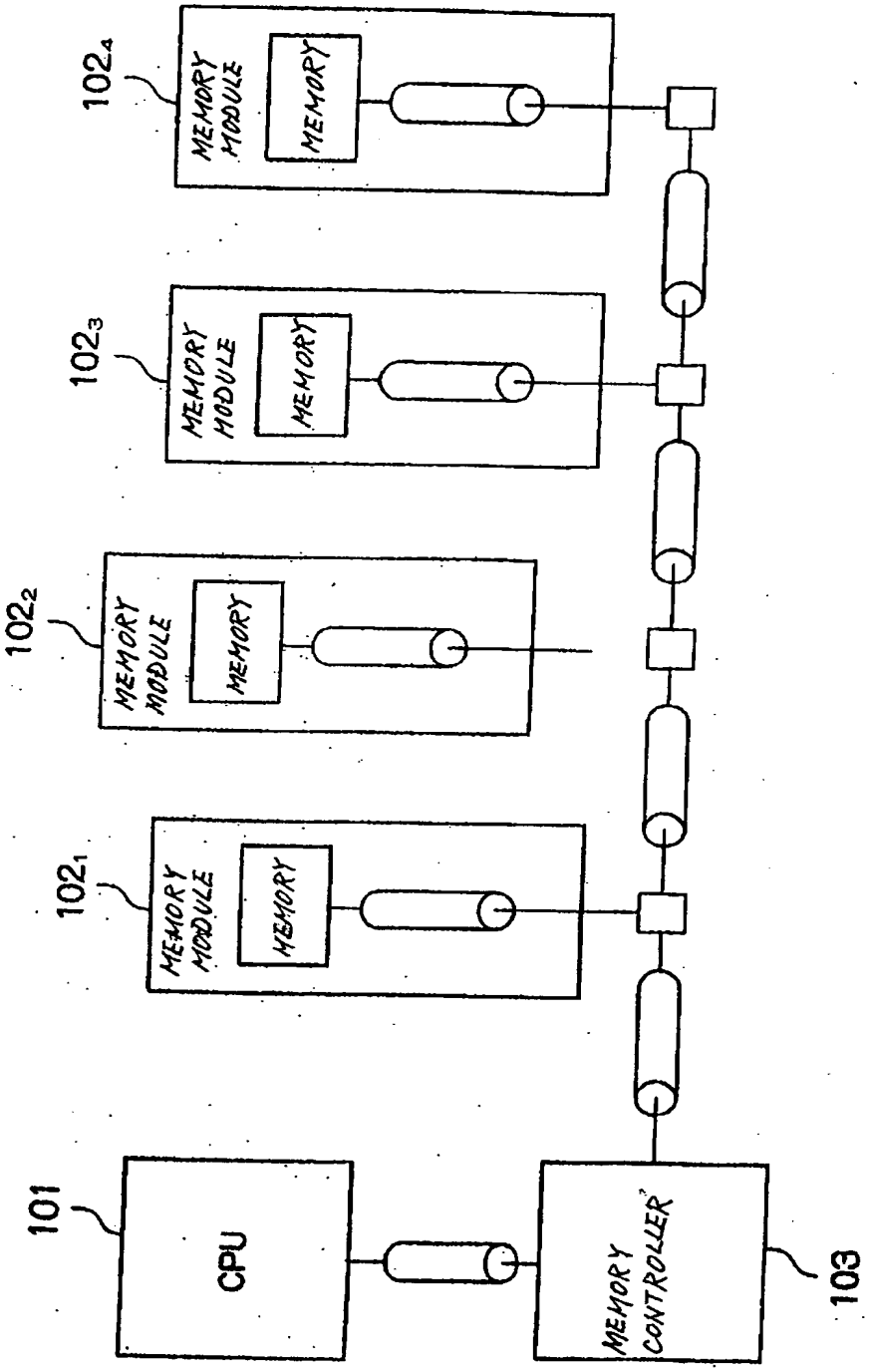


FIG. 1 (PRIOR ART)

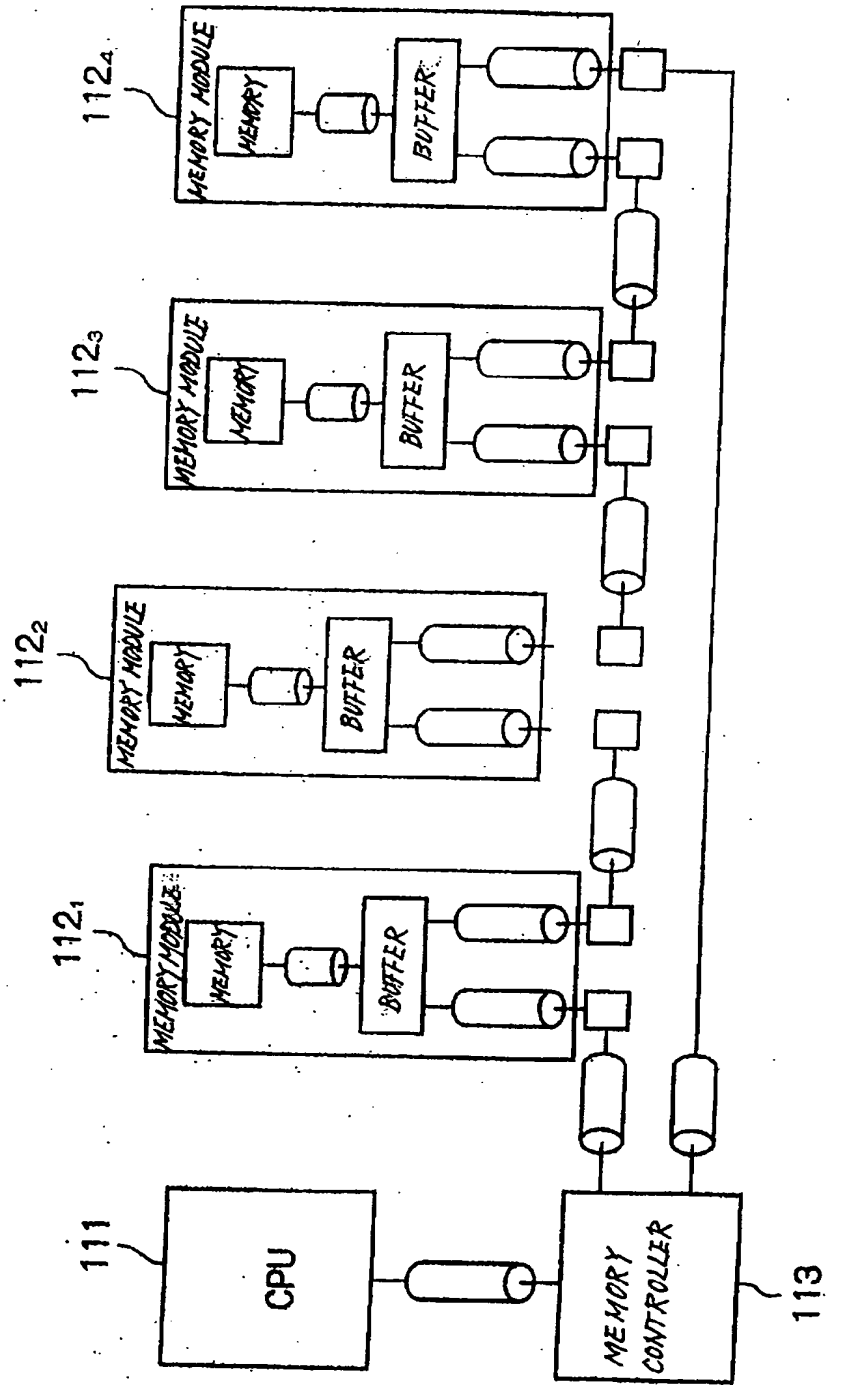


FIG. 2 (PRIOR ART)

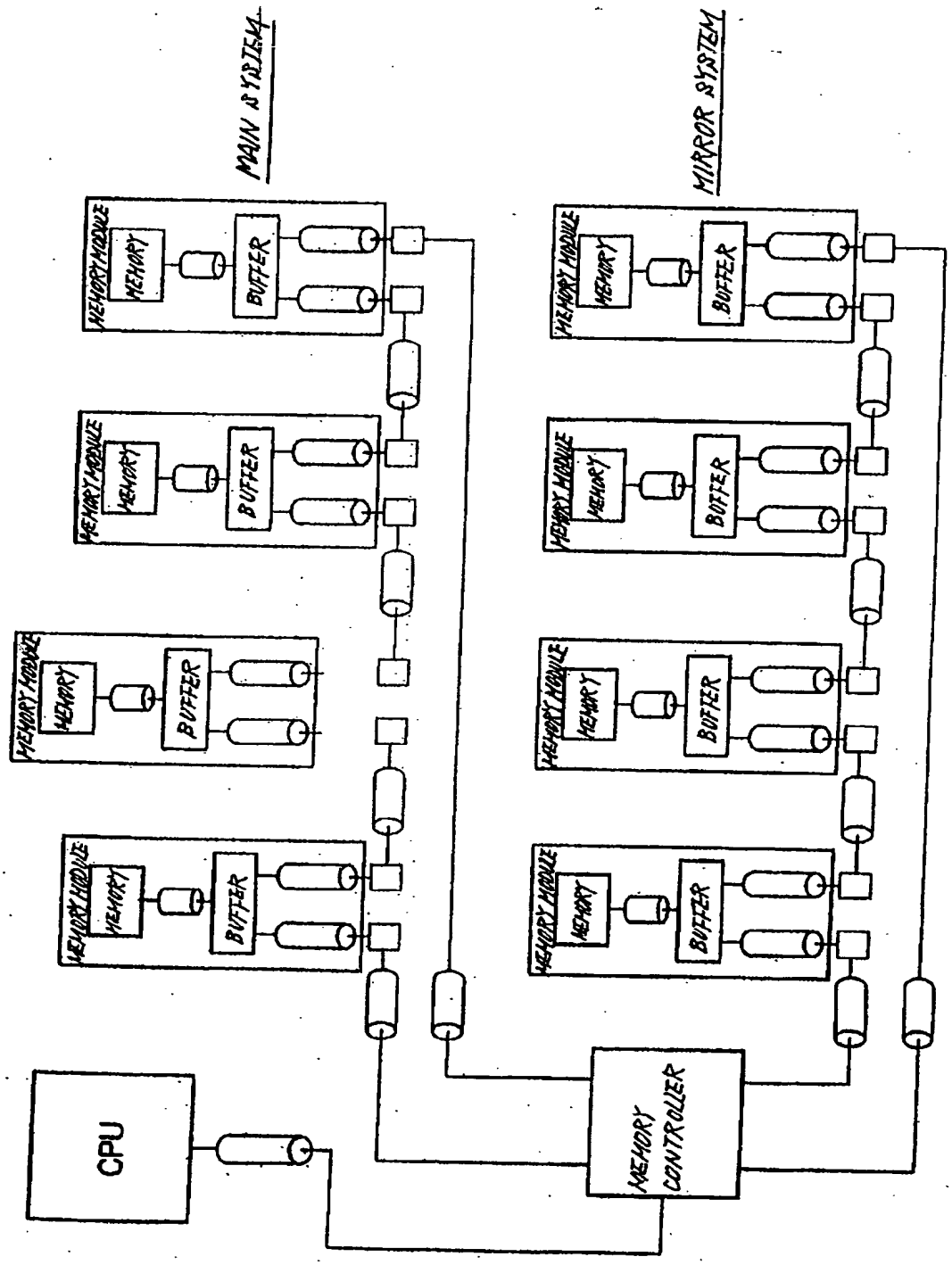


FIG. 3 (PRIOR ART)

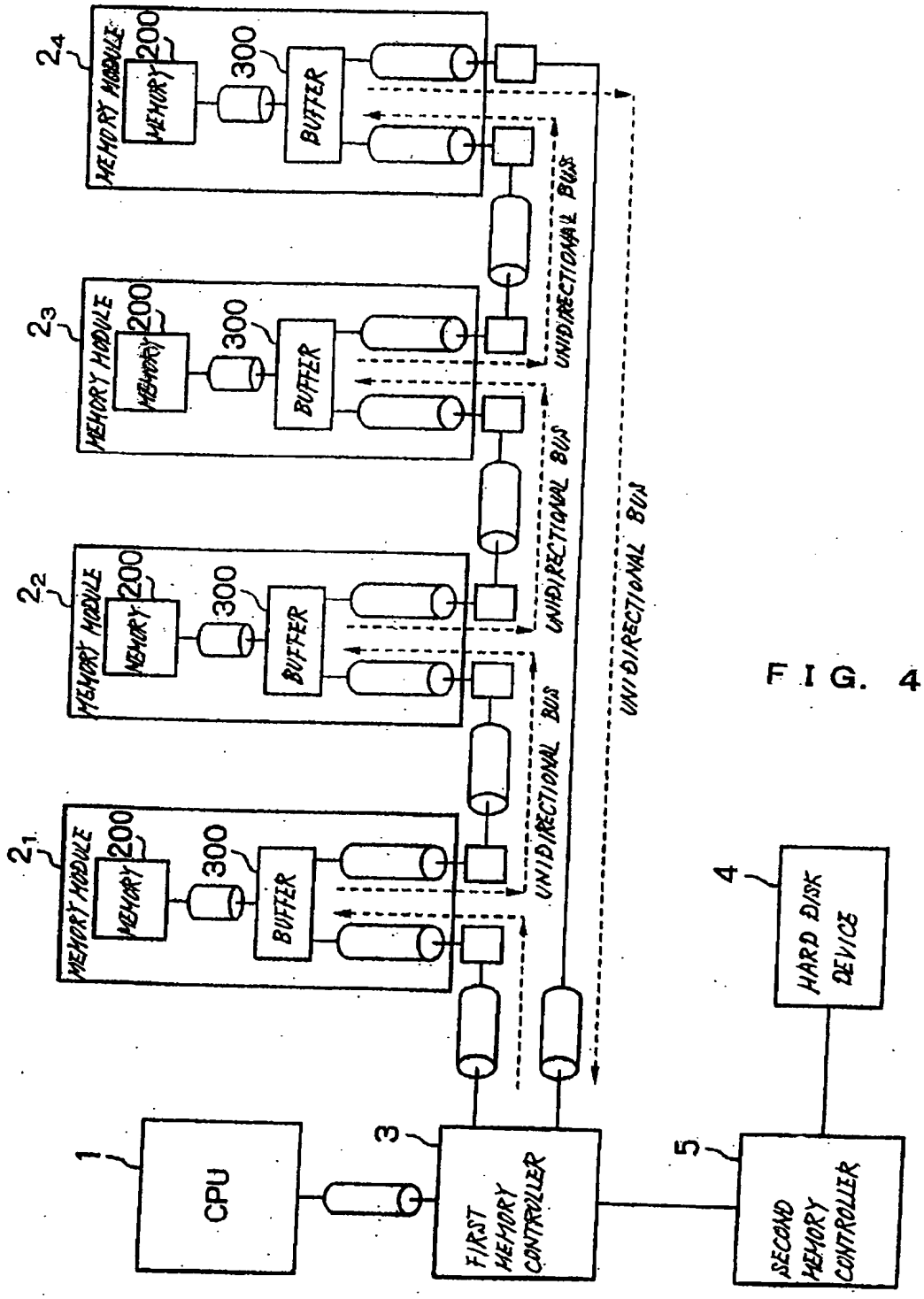

MEMORY MODULE
MEMORY
BUFFER
200
300
2_4
2_3
2_2
2_1
UNIDIRECTIONAL BUS
UNIDIRECTIONAL BUS
UNIDIRECTIONAL BUS
UNIDIRECTIONAL BUS
CPU
1
FIRST MEMORY CONTROLLER
3
SECOND MEMORY CONTROLLER
5
HARD DISK DEVICE
4

FIG. 4

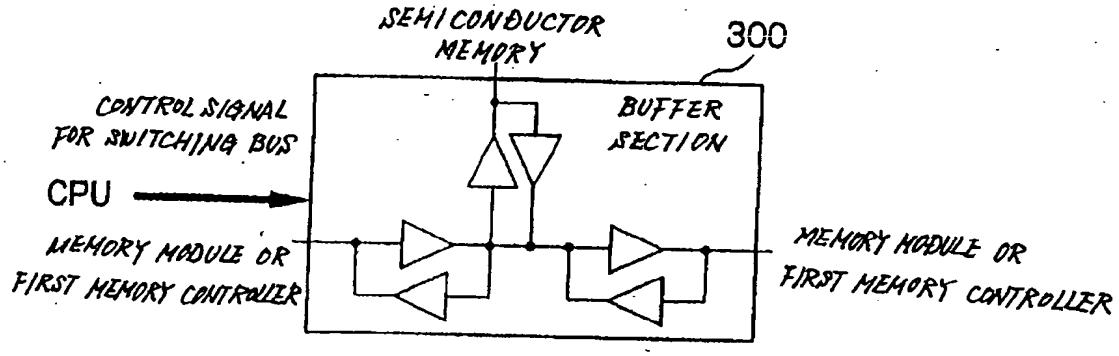


FIG. 5

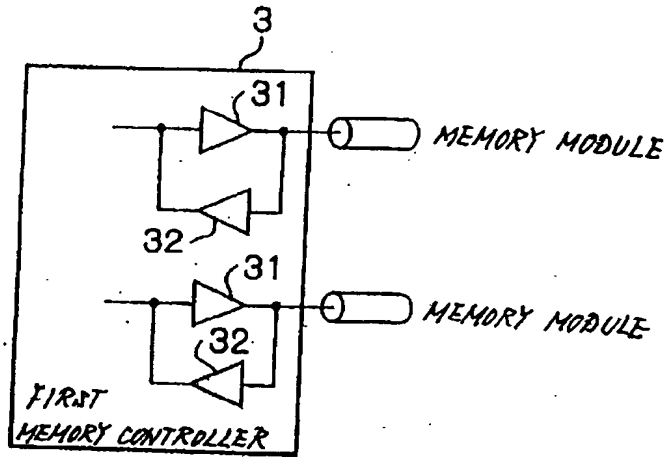


FIG. 6A

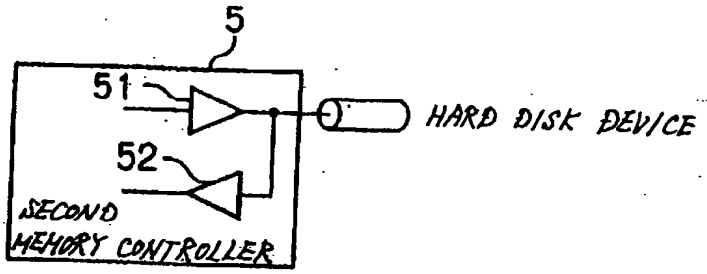


FIG. 6B

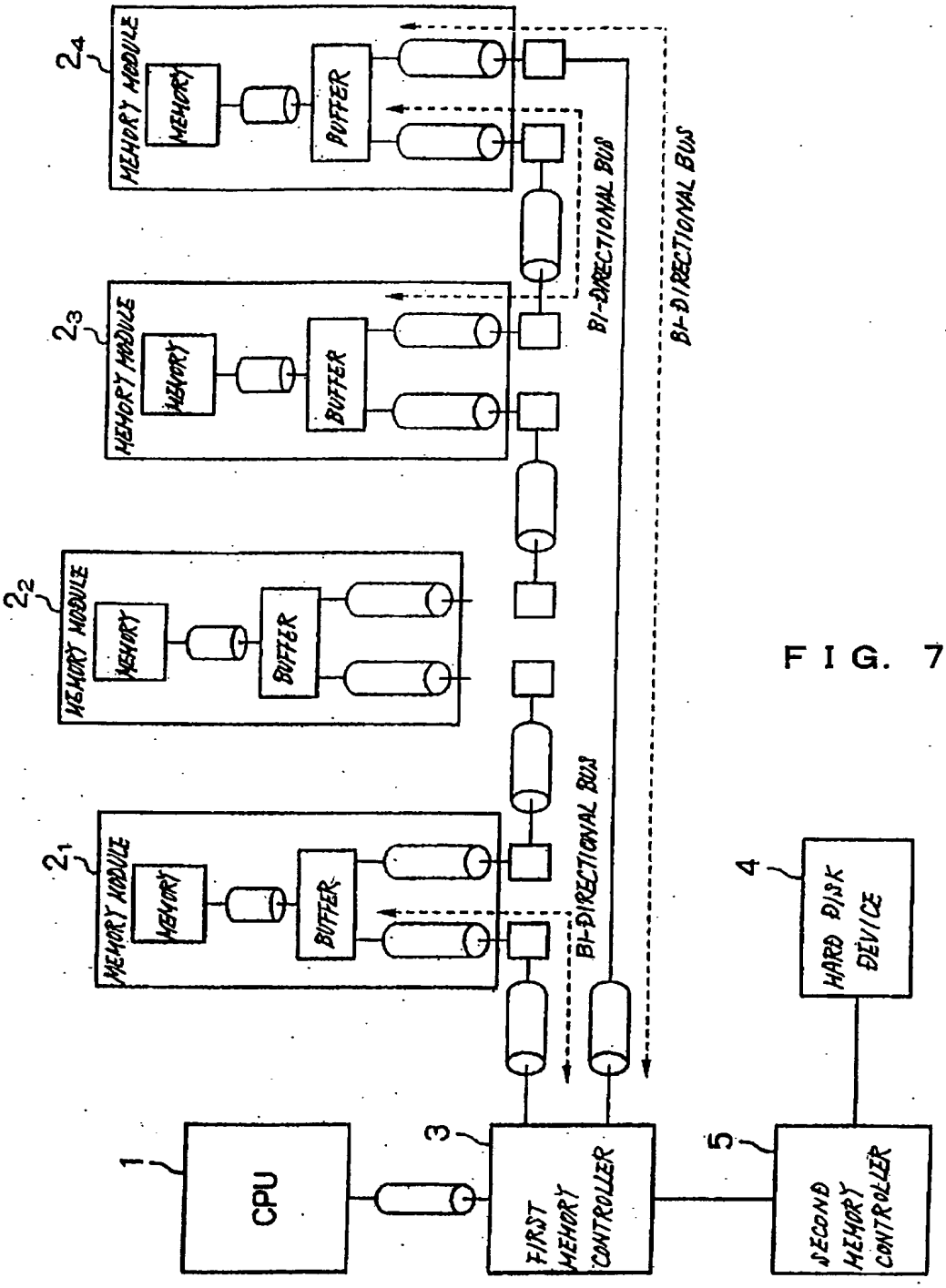

2₄
MEMORY MODULE
MEMORY
BUFFER
2₃
MEMORY MODULE
MEMORY
BUFFER
2₂
MEMORY MODULE
MEMORY
BUFFER
2₁
MEMORY MODULE
MEMORY
BUFFER
BI-DIRECTIONAL BUS
BI-DIRECTIONAL BUS
1
CPU
3
FIRST MEMORY CONTROLLER
5
SECOND MEMORY CONTROLLER
4
HARD DISK DEVICE

FIG. 7

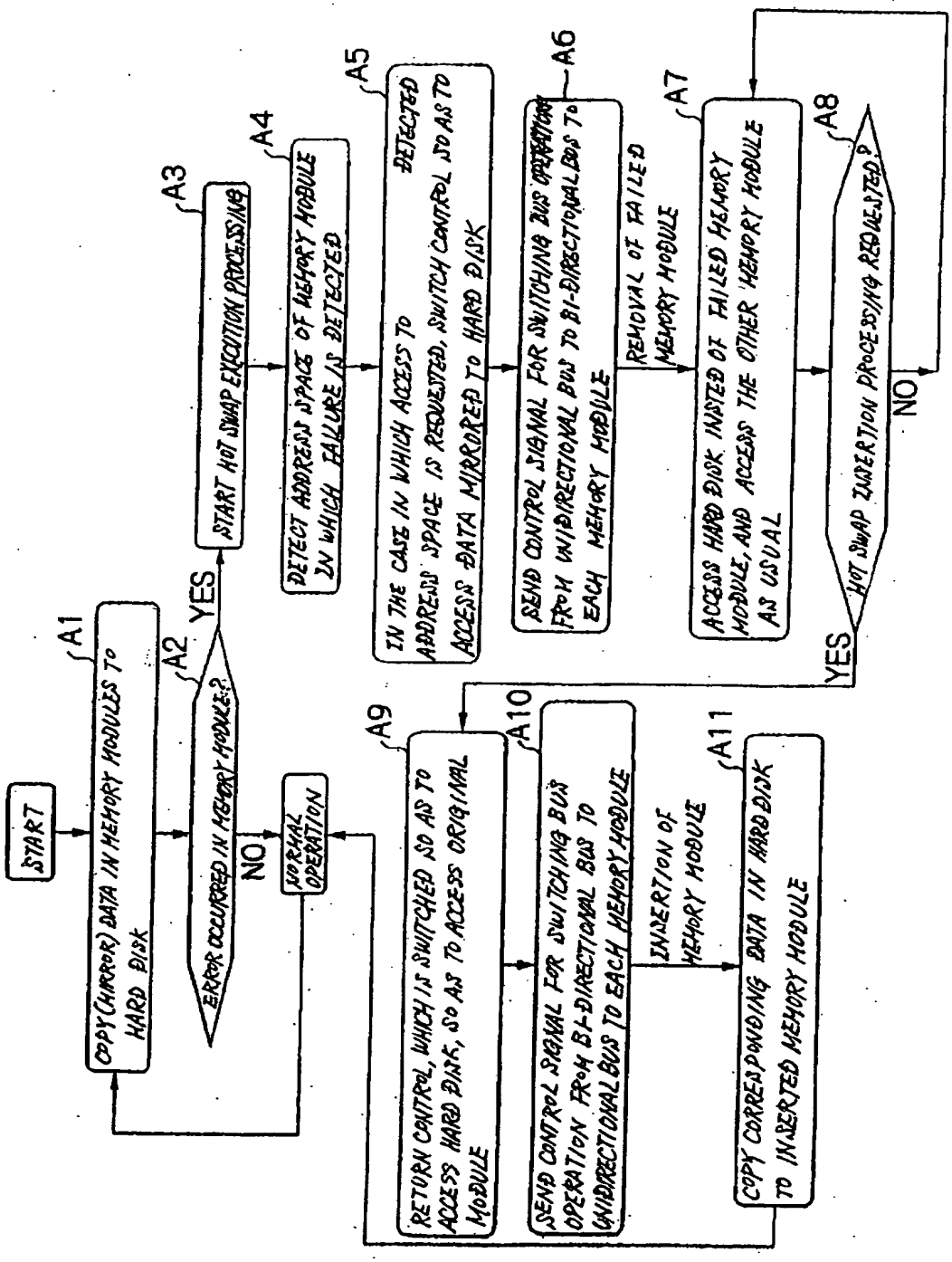

START
A1
COPY (MIRROR) DATA IN MEMORY MODULES TO HARD DISK
A2
ERROR OCCURRED IN MEMORY MODULE?
YES
NO
NORMAL OPERATION
A3
START HOT SWAP EXCUTION PROCESSING
A4
DETECT ADDRESS SPACE OF MEMORY MODULE IN WHICH FAILURE IS DETECTED
A5
IN THE CASE IN WHICH ACCESS TO DETECTED ADDRESS SPACE IS REQUESTED, SWITCH CONTROL SO AS TO ACCESS DATA MIRRORED TO HARD DISK
A6
SEND CONTROL SIGNAL FOR SWITCHING BUS OPERATION FROM UNIDIRECTIONAL BUS TO BI-DIRECTIONAL BUS TO EACH MEMORY MODULE
REMOVAL OF FAILED MEMORY MODULE
A7
ACCESS HARD DISK INSTED OF FAILED MEMORY MODULE, AND ACCESS THE OTHER MEMORY MODULE AS USUAL
A8
HOT SWAP INSERTION PROCESSING REQUESTED?
YES
NO
A9
RETURN CONTROL, WHICH IS SWITCHED SO AS TO ACCESS HARD DISK, SO AS TO ACCESS ORIGINAL MODULE
A10
SEND CONTROL SIGNAL FOR SWITCHING BUS OPERATION FROM BI-DIRECTIONAL BUS TO UNIDIRECTIONAL BUS TO EACH MEMORY MODULE
INSERTION OF MEMORY MODULE
A11
COPY CORRESPONDING DATA IN HARD DISK TO INSERTED MEMORY MODULE

FIG. 8

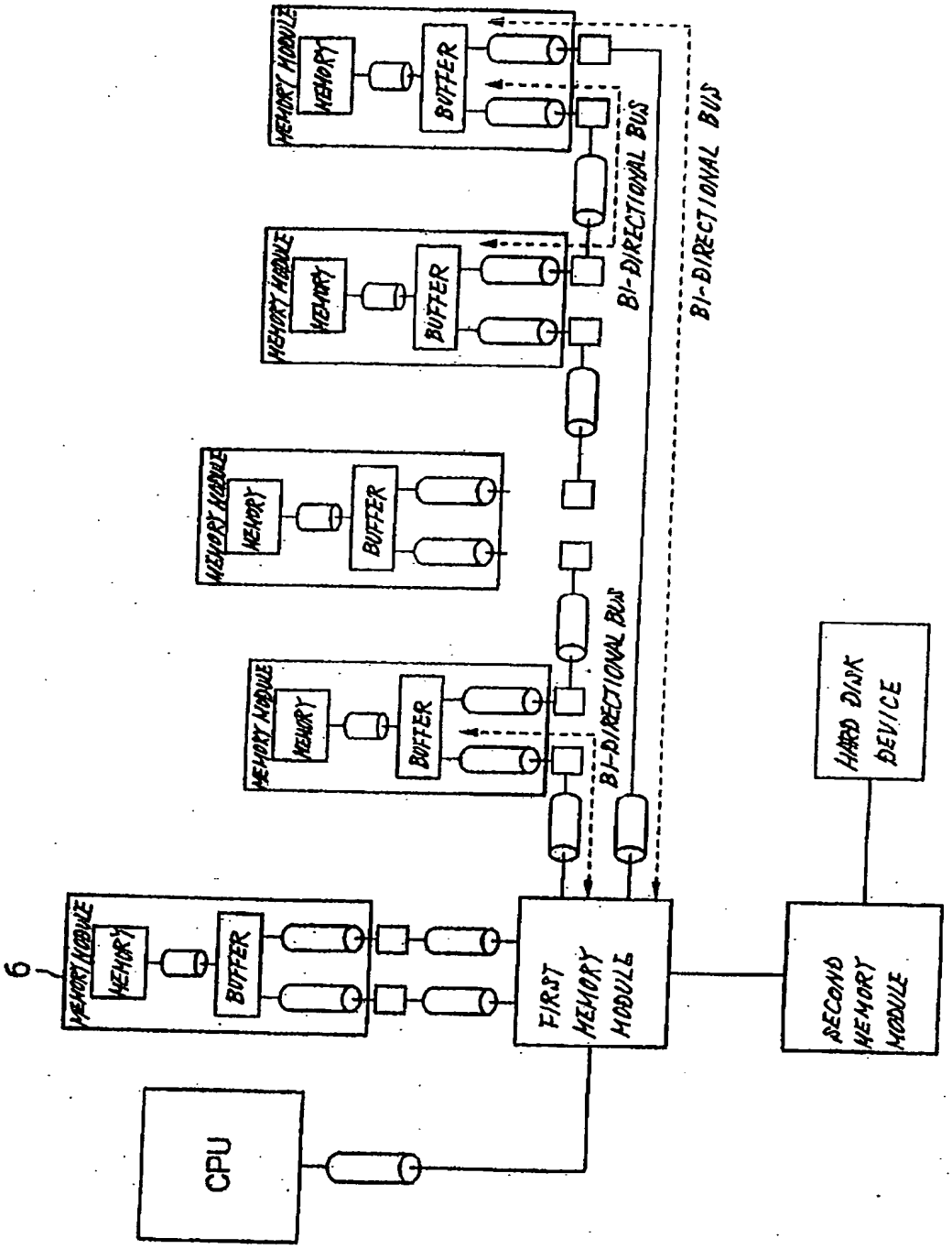

MEMORY MODULE
MEMORY
BUFFER
BI-DIRECTIONAL BUS
BI-DIRECTIONAL BUS
BI-DIRECTIONAL BUS
HARD DISK DEVICE
6
FIRST MEMORY MODULE
SECOND MEMORY MODULE
CPU

FIG. 9

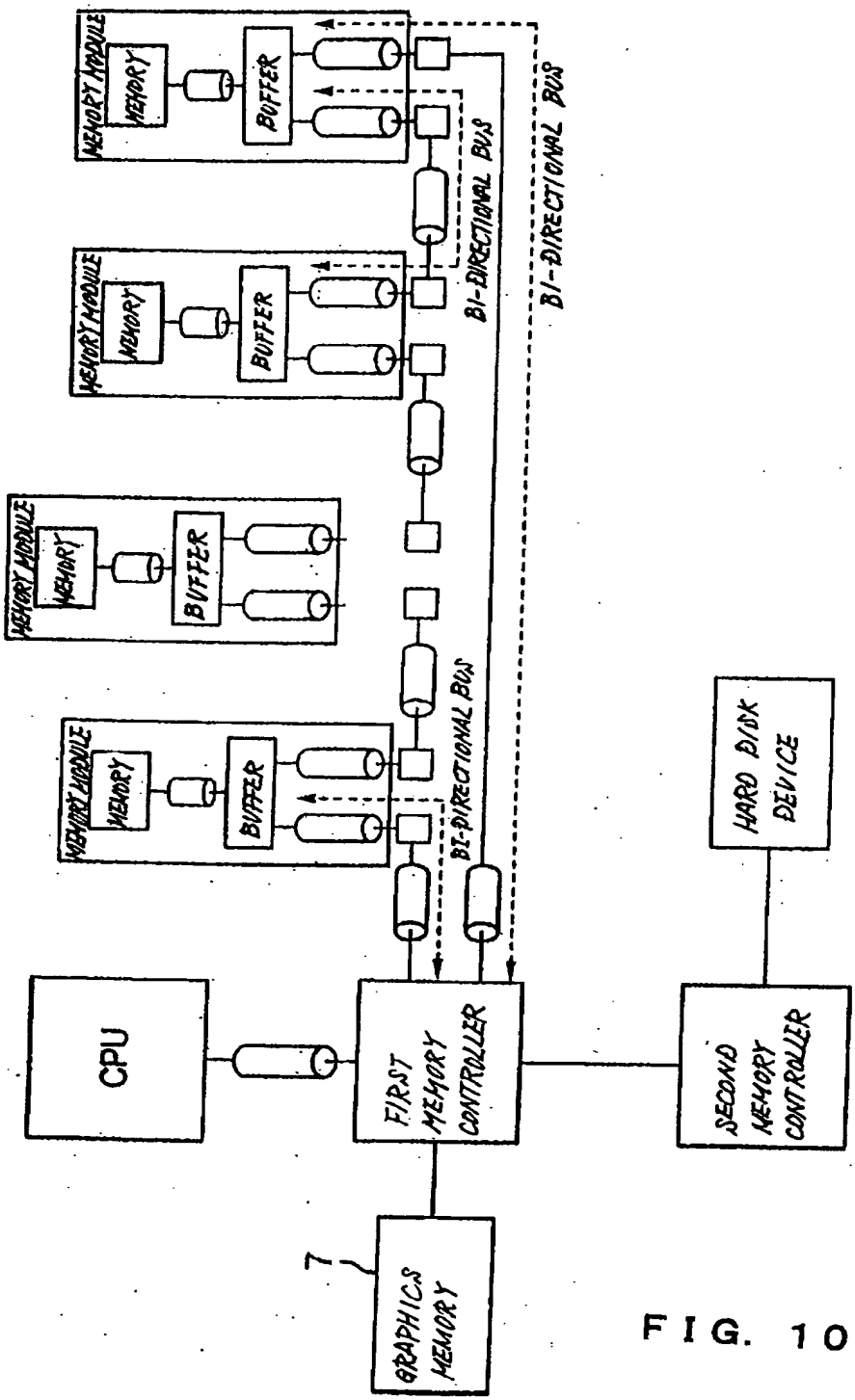

MEMORY MODULE
MEMORY
BUFFER
BI-DIRECTIONAL BUS
BI-DIRECTIONAL BUS
CPU
FIRST MEMORY CONTROLLER
SECOND MEMORY CONTROLLER
HARD DISK DEVICE
7
GRAPHICS MEMORY

FIG. 10

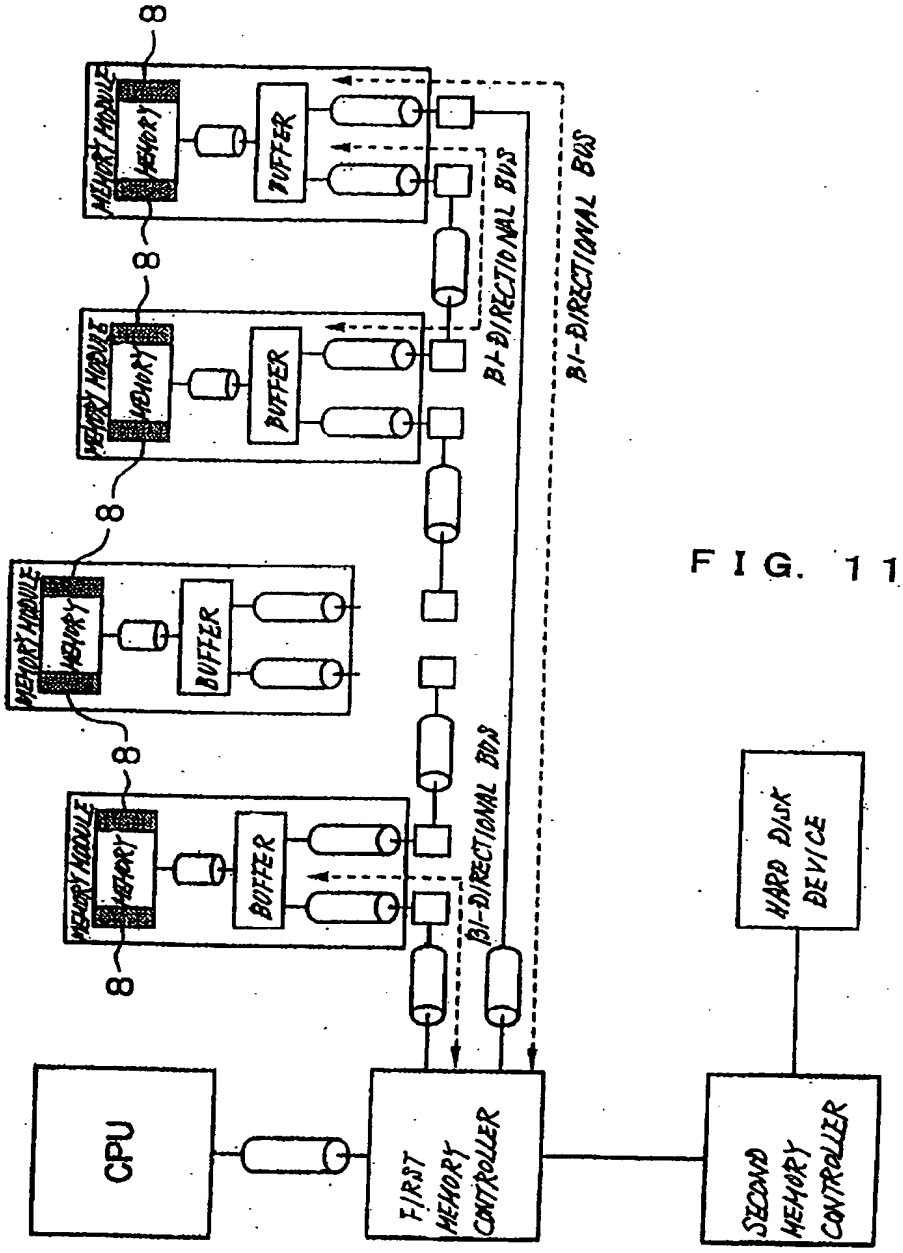

MEMORY MODULE
MEMORY
BUFFER
8
BI-DIRECTIONAL BUS
BI-DIRECTIONAL BUS
CPU
FIRST MEMORY CONTROLLER
SECOND MEMORY CONTROLLER
HARD DISK DEVICE

FIG. 11

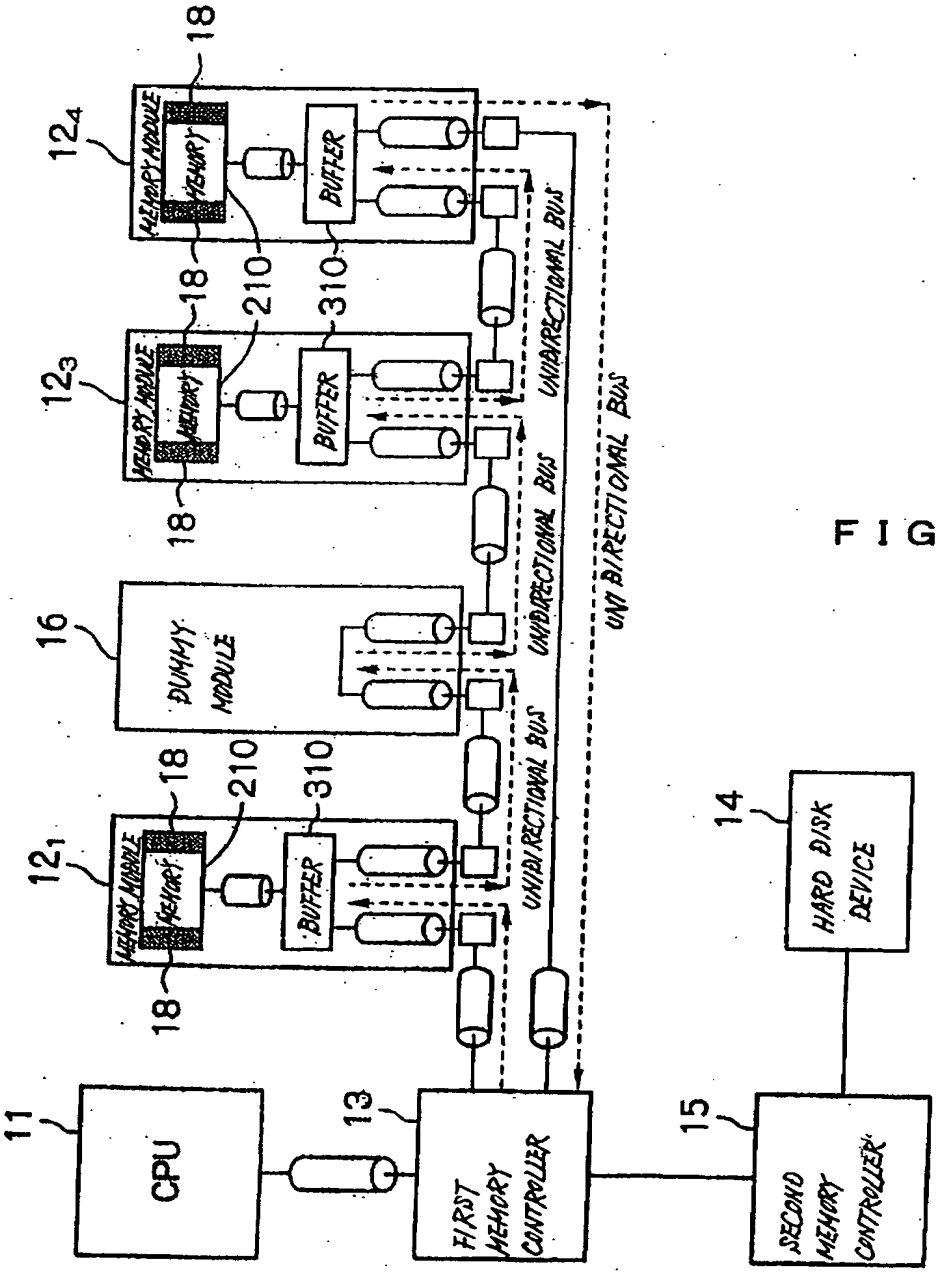

CPU
11
FIRST MEMORY CONTROLLER
13
SECOND MEMORY CONTROLLER
15
HARD DISK DEVICE
14
DUMMY MODULE
16
MEMORY MODULE
MEMORY
BUFFER
18
210
310
12_1
12_3
12_4
UNIDIRECTIONAL BUS
UNIDIRECTIONAL BUS
UNI BIRECTIONAL BUS

FIG. 12

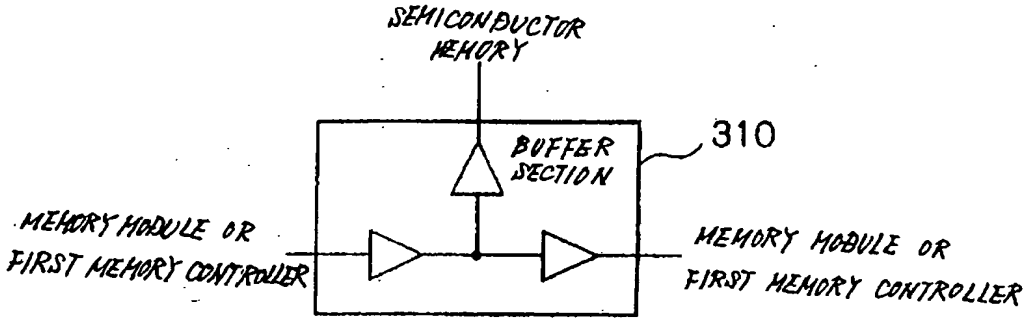


FIG. 13A

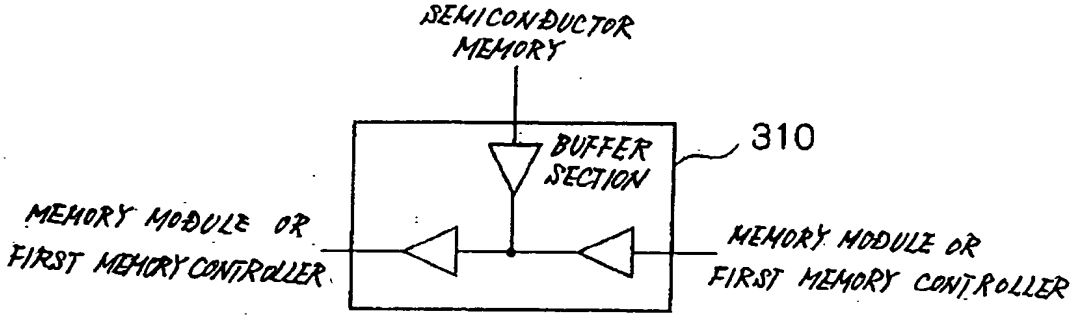


FIG. 13B

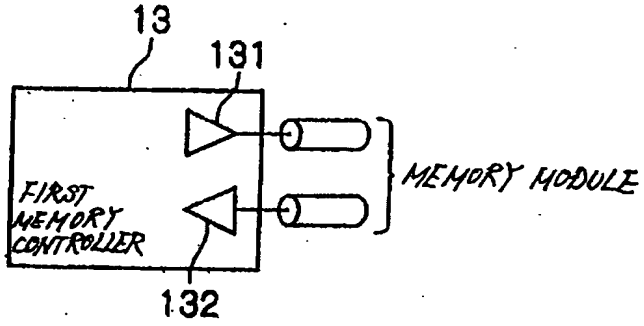


FIG. 14

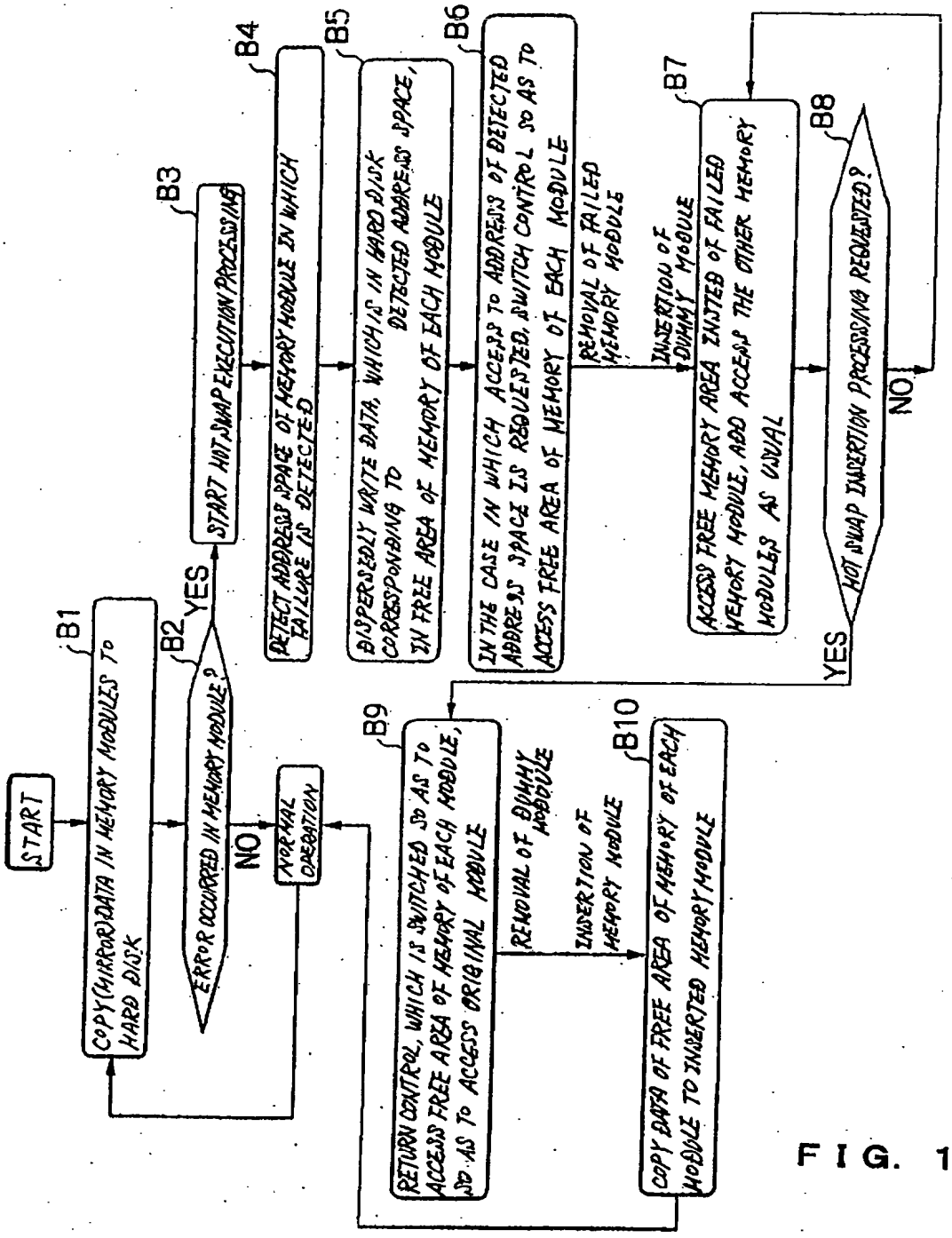

START
B1
COPY(MIRROR)DATA IN MEMORY MODULES TO HARD DISK
B2
ERROR OCCURRED IN MEMORY MODULE?
YES
NO
NORMAL OPERATION
B3
START HOT SWAP EXECUTION PROCESSING
B4
DETECT ADDRESS SPACE OF MEMORY MODULE IN WHICH FAILURE IS DETECTED
B5
DISPERSEDLY WRITE DATA, WHICH IS IN HARD DISK CORRESPONDING TO DETECTED ADDRESS SPACE, IN FREE AREA OF MEMORY OF EACH MODULE
B6
IN THE CASE IN WHICH ACCESS TO ADDRESS OF DETECTED ADDRESS SPACE IS REQUESTED, SWITCH CONTROL SO AS TO ACCESS FREE AREA OF MEMORY OF EACH MODULE
REMOVAL OF FAILED MEMORY MODULE
INSERTION OF DUMMY MODULE
B7
ACCESS FREE MEMORY AREA INSTED OF FAILED MEMORY MODULE, AND ACCESS THE OTHER MEMORY MODULES AS USUAL
B8
HOT SWAP INSERTION PROCESSING REQUESTED?
YES
NO
B9
RETURN CONTROL, WHICH IS SWITCHED SO AS TO ACCESS FREE AREA OF MEMORY OF EACH MODULE, SO AS TO ACCESS ORIGINAL MODULE
REMOVAL OF DUMMY MODULE
INSERTION OF MEMORY MODULE
B10
COPY DATA OF FREE AREA OF MEMORY OF EACH MODULE TO INSERTED MEMORY MODULE

FIG. 15

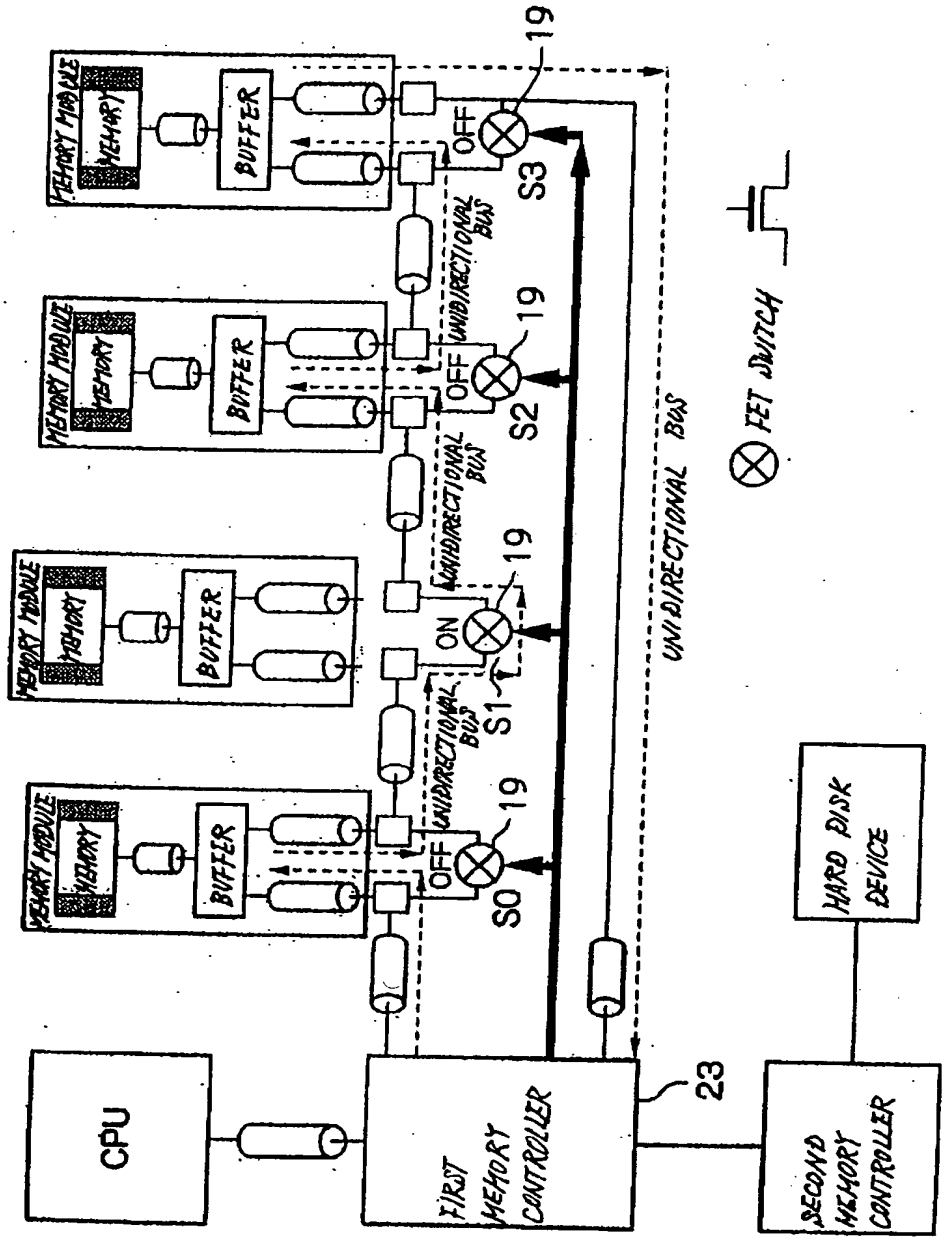
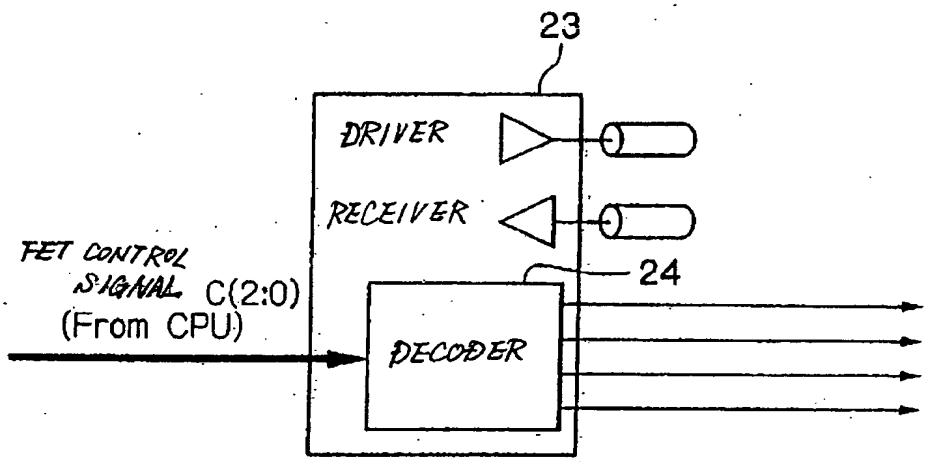

MEMORY MODULE
MEMORY
BUFFER
19
OFF
ON
S3
S2
S1
S0
UNIDIRECTIONAL BUS
FET SWITCH
CPU
FIRST MEMORY CONTROLLER
SECOND MEMORY CONTROLLER
23
HARD DISK DEVICE

FIG. 16



FET CONTROL SIGNAL						
C2	C1	C0	S3	S2	S1	S0
H	L	L	L	L	L	L
L	L	L	L	L	L	H
L	L	H	L	L	H	L
L	H	L	L	H	L	L
L	H	H	H	L	L	L

L : FET SWITCH OFF
H : FET SWITCH ON

FIG. 17

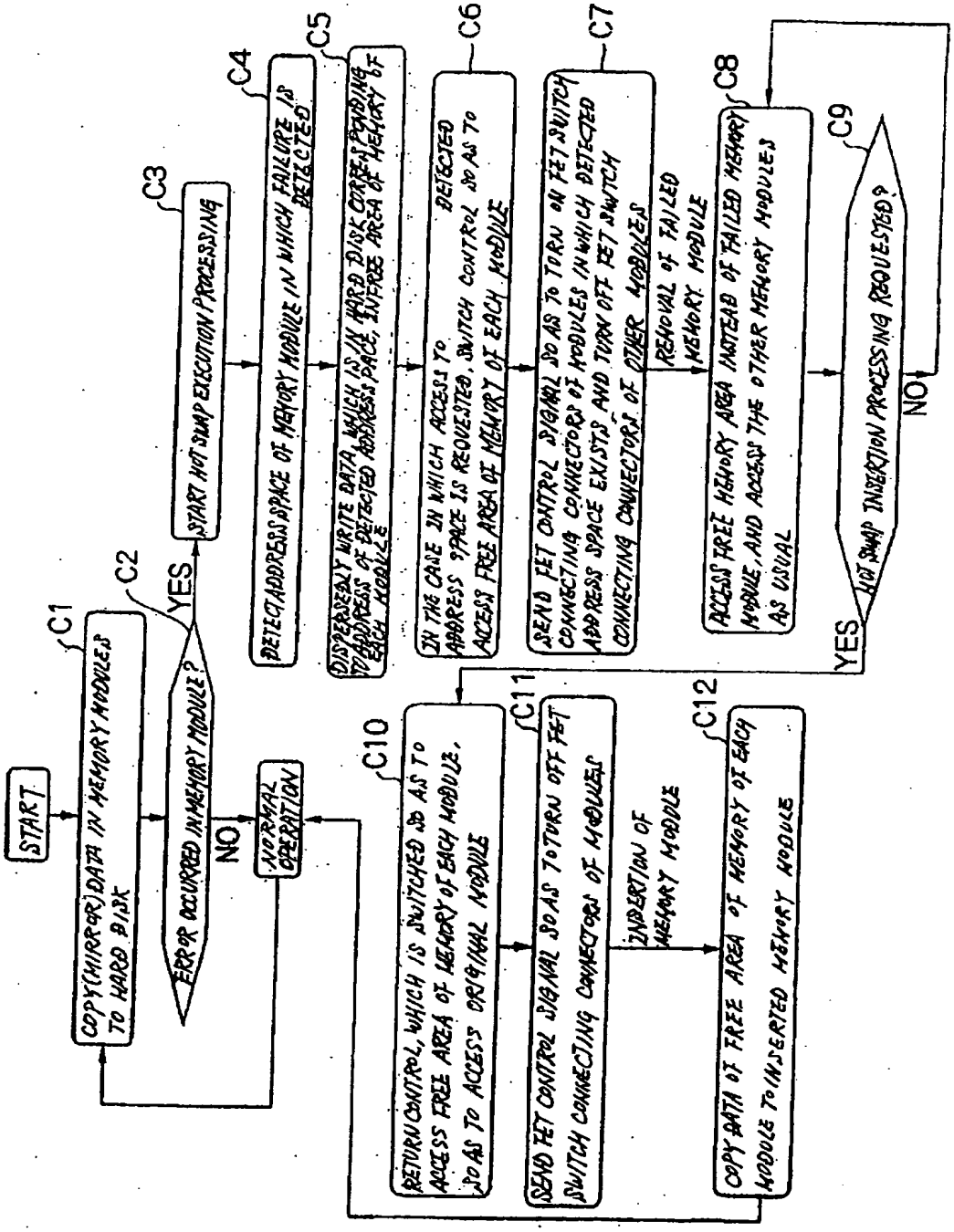

START
C1
COPY(MIRROR) DATA IN MEMORY MODULES TO HARD DISK
C2
ERROR OCCURRED IN MEMORY MODULE?
YES
NO
NORMAL OPERATION
C3
START HOT SWAP EXECUTION PROCESSING
C4
DETECT ADDRESS SPACE OF MEMORY MODULE IN WHICH FAILURE IS DETECTED
C5
DISCRIMINATELY WRITE DATA WHICH IS/IN HARD DISK CORRESPONDING TO ADDRESS OF DETECTED ADDRESS SPACE, INTO FREE AREA OF MEMORY OF EACH MODULE
C6
IN THE CASE IN WHICH ACCESS TO ADDRESS SPACE IS REQUESTED, SWITCH CONTROL SO AS TO ACCESS FREE AREA OF MEMORY OF EACH MODULE
DETECTED
C7
SEND FET CONTROL SIGNAL SO AS TO TURN ON FET SWITCH CONNECTING CONNECTORS OF MODULES IN WHICH DETECTED ADDRESS SPACE EXISTS AND TURN OFF FET SWITCH CONNECTING CONNECTORS OF OTHER MODULES
REMOVAL OF FAILED MEMORY MODULE
C8
ACCESS FREE MEMORY AREA INSTEAD OF FAILED MEMORY MODULE, AND ACCESS THE OTHER MEMORY MODULES AS USUAL
C9
HOT SWAP INSERTION PROCESSING REQUESTED?
YES
NO
C10
RETURN CONTROL, WHICH IS SWITCHED SO AS TO ACCESS FREE AREA OF MEMORY OF EACH MODULE, SO AS TO ACCESS ORIGINAL MODULE
C11
SEND FET CONTROL SIGNAL SO AS TO TURN OFF FET SWITCH CONNECTING CONNECTORS OF MODULES
INSERTION OF MEMORY MODULE
C12
COPY DATA OF FREE AREA OF MEMORY OF EACH MODULE TO INSERTED MEMORY MODULE

FIG. 18

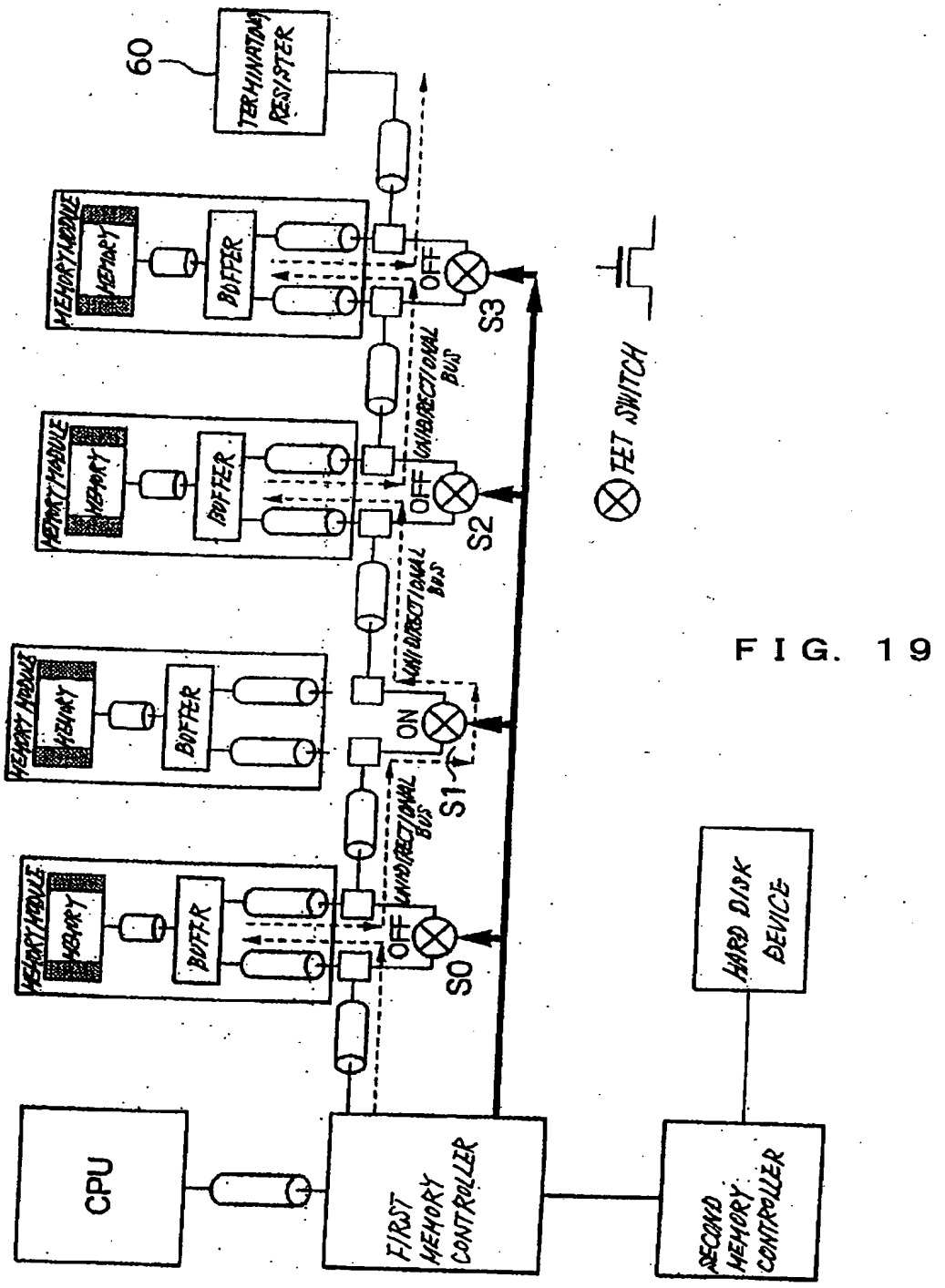
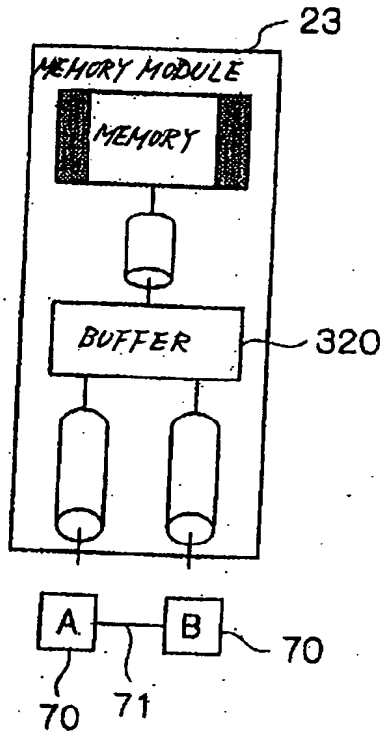

60
TERMINATING RESISTER
MEMORY MODULE
MEMORY
BUFFER
OFF
S3
UNIDIRECTIONAL BUS
S2
ON
S1
S0
FET SWITCH
HARD DISK DEVICE
CPU
FIRST MEMORY CONTROLLER
SECOND MEMORY CONTROLLER

FIG. 19



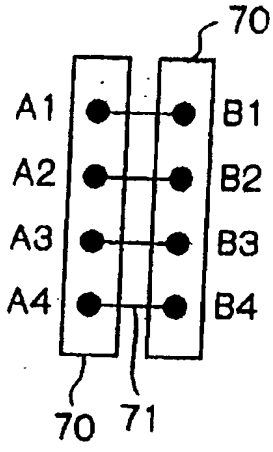


FIG. 20

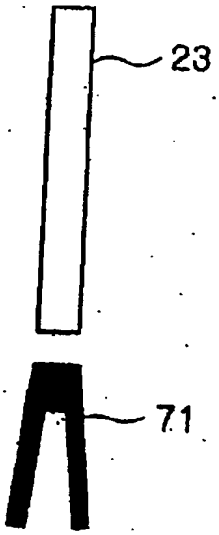


FIG. 21A

FIG. 21B

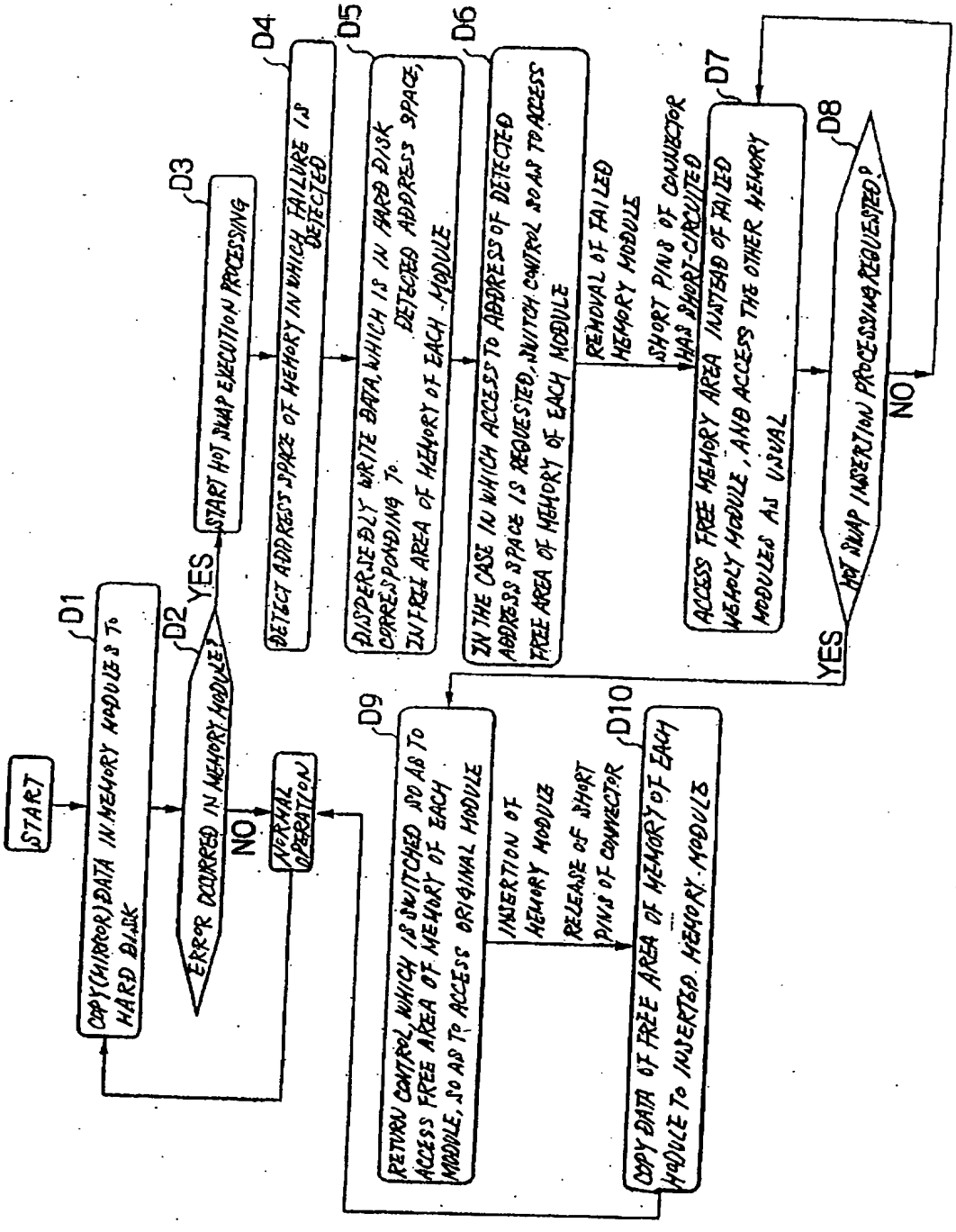

START
D1
COPY(MIRROR) DATA IN MEMORY MODULES TO HARD DISK
D2
ERROR OCCURRED IN MEMORY MODULE?
YES
NO
NORMAL OPERATION
D3
START HOT SWAP EXECUTION PROCESSING
D4
DETECT ADDRESS SPACE OF MEMORY IN WHICH FAILURE IS DETECTED
D5
DISPERSEDLY WRITE DATA WHICH IS IN HARD DISK CORRESPONDING TO DETECTED ADDRESS SPACE, IN FREE AREA OF MEMORY OF EACH MODULE
D6
IN THE CASE IN WHICH ACCESS TO ADDRESS OF DETECTED ADDRESS SPACE IS REQUESTED, SWITCH CONTROL SO AS TO ACCESS FREE AREA OF MEMORY OF EACH MODULE
REMOVAL OF FAILED MEMORY MODULE
SHORT PINS OF CONNECTOR HAS SHORT-CIRCUITED
D7
ACCESS FREE MEMORY AREA INSTEAD OF FAILED MEMORY MODULE, AND ACCESS THE OTHER MEMORY MODULES AS USUAL
D8
HOT SWAP INSERTION PROCESSING REQUESTED?
YES
NO
D9
RETURN CONTROL WHICH IS SWITCHED SO AS TO ACCESS FREE AREA OF MEMORY OF EACH MODULE, SO AS TO ACCESS ORIGINAL MODULE
INSERTION OF MEMORY MODULE
RELEASE OF SHORT PINS OF CONNECTOR
D10
COPY DATA OF FREE AREA OF MEMORY OF EACH MODULE TO INSERTED MEMORY MODULE

FIG. 22